3. System Module

Contents

Transceiver NPW-2NX

Introduction

The NPW-2NX is a dual band transceiver unit designed for the TDMA800/1900 networks.

The transceiver consists of engine module (LN8) and assembly parts.

The transceiver has a full graphic display and the user interface is based on the Jack 3 UI with two soft keys.

An internal antenna is used, there is no connection to an external antenna.

The transceiver has a low leakage tolerant earpiece and an omnidirectional microphone, providing excellent audio quality.

An integrated IR link provides a connection between two NPW-2 transceivers or a transceiver and a PC (internal data), or a transceiver and a printer.

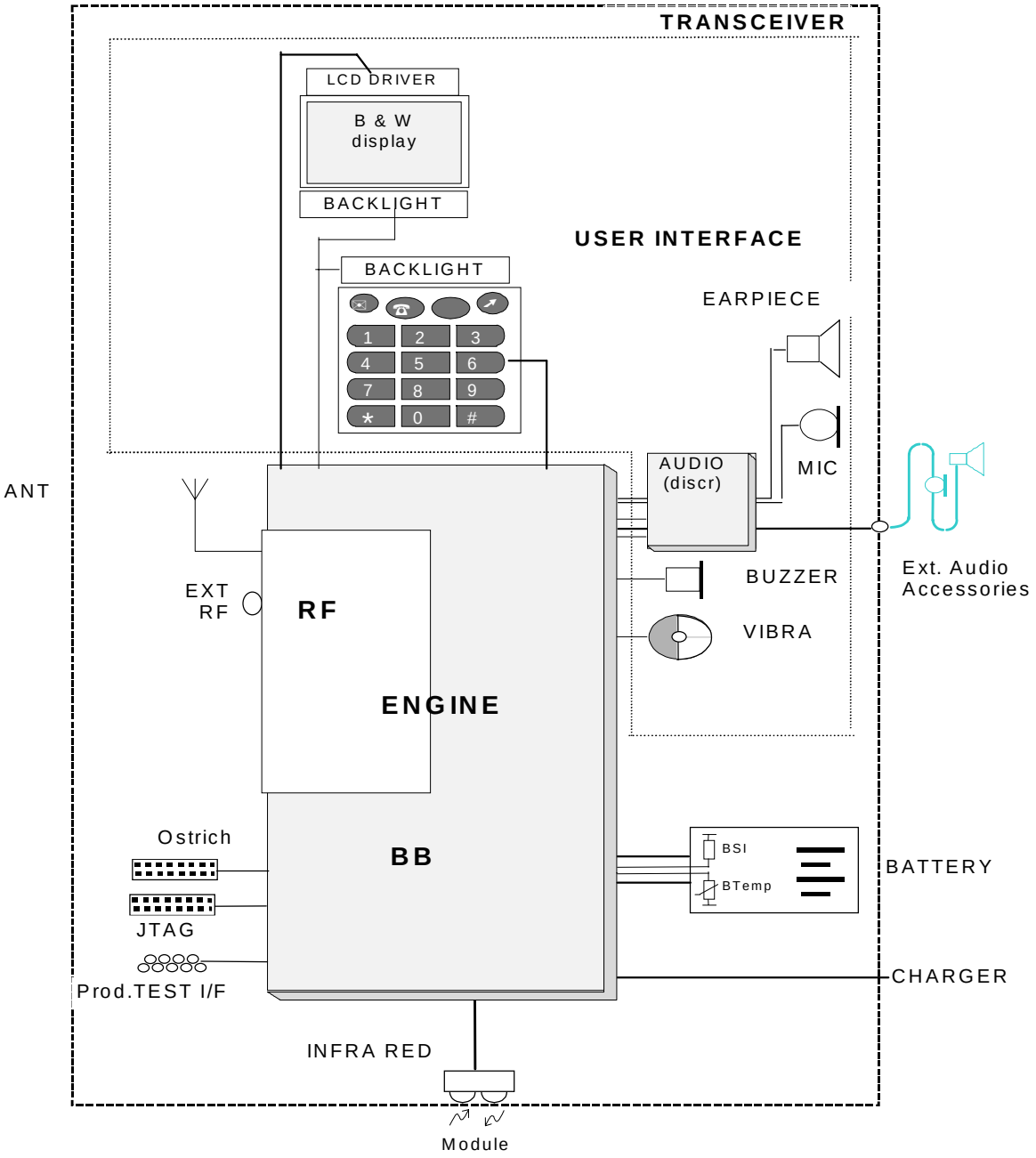

Figure 1: Interconnecting Diagram.

Operational Modes

There are several different operational modes. Modes have different states controlled by the cellular SW. Some examples are: Idle State (on ACCH), Camping (on DCCH), Scanning, Conversation, No Service Power Save (NSPS) *previously OOR = Out of Range*.

In the power off mode, only the circuits needed for power up are supplied.

In the idle mode, circuits are powered down and only the sleep clock is running.

In the active mode, all the circuits are supplied with power although some parts might be in idle state part of the time.

The charge mode is effective in parallel with all previous modes. The charge mode itself consists of two different states (*i.e.*, the fast charge and the maintenance mode).

The local mode is used for alignment and testing.

Engine Module

Environmental Specifications

Normal and extreme voltages

Voltage range:

- nominal battery voltage: 3.6 V
- maximum battery voltage: 5.0 V
- minimum battery voltage: 3.1 V

Temperature Conditions

Temperature range:

- ambient temperature: -30...+ 60 °C
- PWB temperature: -30...+85 °C

Baseband Module

The core part of 6360 BB consists of two ASICs—UEM and UPP—and flash memory. The Following sections describe these parts.

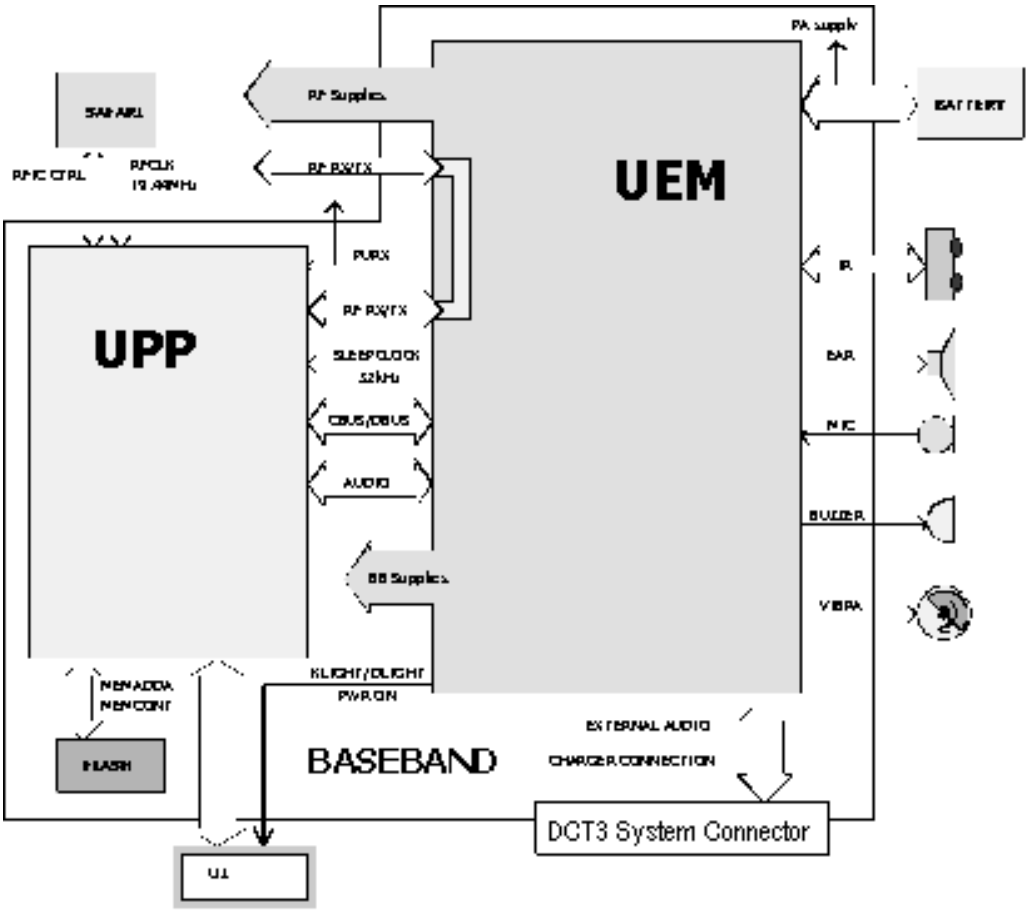

Figure 2: System Block Diagram (simple).

UEM

UEM introduction

The UEM is the Universal Energy Management IC for DCT4 digital handportable phones. In addition to energy management, it performs all the baseband mixed-signal functions.

Most UEM pins have 2kV ESD protection and those signals which are considered to be exposed more easily to ESD have 8kV protection inside UEM. Such signals are all audio signals, headset signals, BSI, Btemp, Fbus, and Mbus signals.

Regulators

The UEM has six regulators for BB power supplies and seven regulators for RF power supplies. The VR1 regulator has two outputs (VR1a and VR1b). In addition, there are two current generators (IPA1 and IPA2) for biasing purposes.

A bypass capacitor (1uF) is required for each regulator output to ensure stability.

Reference voltages for regulators require external 1uF capacitors. Vref25RF is reference voltage for VR2 regulator, Vref25BB is reference voltage for VANA, VFLASH1, VFLASH2, VR1 regulators, Vref278 is reference voltage for VR3, VR4, VR5, VR6, VR7 regulators, VrefRF01 is reference voltage for VIO, VCORE, VSIM regulators, and for RF.

BB	RF	Current
VANA: 2.78Vtyp 80mAmax	VR1a:4.75V 10mAmax VR1b:4.75V	IPA1: 0-5mA
Vflash1: 2.78Vtyp 70mAmax		IPA2: 0-5mA
Vflash2: 2.78Vtyp 40mAmax	VR2:2.78V 100mAmax	
VSim: 1.8/3.0V 25mAmax	VR3:2.78V 20mA	
VIO: 1.8Vtyp 150mAmax	VR4: 2.78V 50mAmax	
Vcore: 1.0-1.8V 200mAmax	VR5: 2.78V 50mAmax	
	VR6: 2.78V 50mAmax	
	VR7: 2.78V 45mAmax	

VANA regulator supplies internal and external analog circuitry of BB. It is disabled in sleep mode.

Vflash1 regulator supplies LCD, IR-module and digital parts of UEM and Safari asic. It is enabled during startup and goes to low Iq-mode in sleep mode.

Vflash2 regulator supplies data cable (DLR-3). It's enabled/disenabled through writing GENIO(0&2) in the UPP; the default is off.

VIO regulator supplies both external and internal logic circuitries. It's used by LCD, flash, and UPP. Regulator goes in to low Iq-mode in sleep mode.

VCORE regulator supplies DSP and Core part of UPP. Voltage is programmable and the start-up default is 1.5V. Regulator goes to low Iq-mode in sleep mode.

VSIM regulator supplies SIM card. Voltage is programmable. Regulator goes in to low Iq-mode in sleep mode.

VR1 regulator uses two LDOs and a charge pump. Charge pump requires one external 1uF capacitor in Vpump pin and 220nF flying capacitor between pins CCP and CCN. In practice, 220nF flying capacitor is built by 2 x 100nF capacitors in parallel. VR1 regulator is used by Safari RF ASIC.

VR2 regulator is used to supply external RF parts, lower band up converter, TX power detector module, and Safari. In light load situations, VR2 regulator can be set to low Iq-mode.

VR3 regulator supplies VCTCXO and Safari in RF. It's always enabled when UEM is active. When UEM is in sleep mode, VR3 is disabled.

VR4 regulator supplies RF parts having low noise requirements. In light load situations, VR4 regulator can be set to low Iq-mode.

VR5 regulator supplies lower band PA. In light load situations, VR5 regulator can be set to low Iq-mode.

VR6 regulator supplies higher band PA and TX amplifier. In light load situations, VR6 regulator can be set to low Iq-mode.

VR7 regulator supplies VCO and Safari. In light load situations, the VR7 regulator can be set to low Iq-mode.

IPA1 and IPA2 are programmable current generators. 27kW/1%/100ppm external resistor is used to improve the accuracy of output current. IPA1 is used by lower band PA and IPA2 is used by higher band PA.

RF Interface

The interface between the baseband and the RF section also is handled by UEM. It provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the UI section. The UEM supplies the analog AFC signal to RF section according to the UPP DSP digital control. It also converts PA & VCTCXO temperature into real data for the DSP.

Charging Control

The CHACON block of UEM asics controls charging. Needed functions for charging controls are pwm-controlled battery charging switch, charger-monitoring circuitry, and battery voltage monitoring circuitry. In addition, external components are needed for EMC protection of the charger input to the baseband module. The DCT4 baseband is designed to support both DCT3 and DCT4 chargers from an electrical point of view.

Digital Interface

Data transmission between the UEM and the UPP is implemented using two serial connections, DBUS (programmable clock) for DSP and CBUS (1.0MHz GSM and 1.08MHz TDMA) for MCU. UEM is a dual voltage circuit, the digital parts are running from 1.8V and the analog parts are running from 2.78V. Vbat (3,6V) voltage regulator inputs also are used.

Audio Codec

The baseband supports two external microphone inputs and one external earphone output. The inputs can be taken from an internal microphone, from a headset microphone, or from an external microphone signal source through headset connector. The output for the internal earpiece is a dual-ended type output, and the differential output is capable of driving 4Vpp to the earpiece with a 60 dB minimum signal to total distortion ratio. Input and output signal source selection and gain control is performed inside the UEM

Asic according to control messages from the UPP. The buzzer and an external vibra alert control signals are generated by the UEM with separate PWM outputs.

UI Drivers

There are discrete drivers for the buzzer, vibra, display, and keyboard LEDs, and IR inside UEM. These generate a PWM square wave to devices.

IR Interface

The IR interface is designed into the UEM. The low frequency mode of IR module covers speed up to 115.2 kbit/s. The device (Vishay) tranceivers integrate a sensitive receiver and a built-in power driver. The inputs (Txd, SD/Mode) and the output (Rxd) are directly coupled to the I/O circuit. VBAT gives power supply to the transmit LED and serial resistor limits current. Received infrared data to IR LED goes straight to UEM by RXD line. Vflash1 is the power supply of the IR module transmit. The IR module has one control pin to control shut down. Control lever shifter is used to change proper voltage to IR module from UPP for shutdown.

AD Converters

There is an 11-channel analog-to-digital converter in UEM. The AD converters are calibrated in the production line.

Introduction

NPW-2 uses UPPv8MB ASIC. The RAM size is 8M. The UPP ASIC is designed to operate in a DCT4 engine. The UPP processor architecture consists of both DSP and MCU processors.

Blocks

UPP is internally partitioned into two main parts:

The Processor and Memory System (*i.e.,* Processor cores, Mega-cells, internal memories, peripherals, and external memory interface). This is known as the Brain.

The Brain consists of the blocks: the DSP Subsystem (DSPSS), the MCU Subsystem (MCUSS), the emulation control (EMUCtl), the program/data RAM (PDRAM) and the Brain Peripherals–subsystem (BrainPer).

The NMP custom cellular logic functions. This is known as the Body.

The Body contains all interfaces and functions needed for interfacing other DCT4 baseband and RF parts. Body consists of following sub-blocks: MFI, SCU, CTSI, RxModem, AccIF, UIF, Coder, GPRSCip, BodyIF, SIMIF, PUP, and CDMA (Corona).

Flash Memory

Introduction

The NPW-2NX tranceiver uses a 64-Mbit flash as its external memory. The VIO regulator is used as a power supply for normal in-system operation. An accelerated program/erase operation can be obtained by supplying Vpp of 12 volt to the flash device.

The device has two read modes: asynchronous and burst. The Burst read mode is utilized

in NPW-2, except for the start-up, when the asynchronous read mode is used for a short time.

In order to reduce the power consumpition on the bus, a Power Save function is introduced. This reduces the amount of switching on the external bus.

User Interface Hardware

LCD

Introduction

NPW-2 uses a black-and-white GD51 96 x 65 full dot matrix graphical display. The LCD module includes LCD glass, LCD COG-driver, elastomer connector, and metal frame. The LCD module is included with the lightguide assembly module.

Interface

SW and the control signals are from the UPP asic. The VIO and Vflash1 regulators supply the LCD with power. The LCD has an internal voltage booster and a booster capacitor is required between Vout and GND.

Pin 3 (Vss9) is the LCD driver's ground and Pin 9 (GND) is used to ground the metal frame. LCD is controlled by UI SW and control signals.

Booster capacitor (C302 100nF) is connected between booster pin (Vout) and ground. The capacitor stores boosting voltage.

Pin 9 (GND) is the metal frame ground pin so it is not coming from the display driver.

Keyboard

Introduction

The NPW-2NX keyboard follows the Jack III style with side keys for volume control.

PWR key is integrated so that it is part of IR window and located on top of phone.

Power Key

All keyboard signals come from UPP asic, except pwr key signal, which is connected directly to UEM. Pressing of pwr key is detected so that switch of pwr key connects PWONX is of UEM to GND and creates an interrupt.

Keys

As keys other than the power key are pressed, the metal dome connects one S-line and one R-line of UPP. A SW interrupt is created. The matrix of how lines are connected and which lines are used for different keys is described in the following table. S-line S0 and

R-line R5 are not used.

Returns / Scans	S0	S1	S2	S3	S4
R0	Volume up side key	NC	Send	End	NC
R1	Volume down side key	Soft left	Up	Down	Soft right
R2	NC	1	4	7	*
R3	NC	2	5	8	0
R4	NC	3	6	9	#
R5	NC	NC	NC	NC	NC

NC = Not Connected

Lights

Introduction

NPW-2 has LEDs for lighting purposes: six LEDs for keyboard and four LEDs for display. LED type is LGM470 (green).

Interfaces

Display lights are controlled by the Dlight signal from UEM. Dlight output is a PWM (Pulse Width Modulation) signal, which is used to control average current going through LEDs. When battery voltage changes, a new PWM value is written to the PWM register. This ensures that brightness of lights remains the same with all battery voltages. Frequency of the signal is fixed 128Hz.

Keyboard lights are controlled by Klight signal from UEM. Klight output is a PWM signal and is similar to Dlight.

Technical Information

LED locates in hole and terminals are soldered on the component side of the module PWB. The LEDs have a white plastic body around the diode, and this directs the emitted light better to the UI-side.

The current for the LCD lights is limited by the resistor between the Vbatt and LEDs. For the keyboard lights, there are resistors in parallel.

Vibra

Introduction

The vibra is located on D-cover and is connected by spring connectors on PWB. It is located in the left bottom side of the engine.

Interfaces

The vibra is controlled by the PWM signal VIBRA from the UEM. With this signal, it is

possible to control both the frequency and pulse width of signal. Pulse width is used to control current when the battery voltage changes. Frequency control makes it possible to search for an optimum frequency to provide silent and efficient vibrating.

Audio Hardware

Earpiece

Introduction

The 13 mm speaker capsule that is used in DCT3 products is also used in NPW-2NX.

The speaker is dynamic. It is very sensitive and capable of producing relatively high sound pressure at low frequencies.

Microphone

Introduction

The microphone is an electret microphone with an omnidirectional polar pattern. It consists of an electrically polarized membrane and a metal electrode which forms a capacitor. Air pressure changes (*i.e.*, sound) move the membrane, which cause voltage changes across the capacitor. Becauce the capacitance is typically 2 pF, a FET buffer is needed inside the microphone capsule for the signal generated by the capacitor. Because of the FET, the microphone requires a bias voltage.

Buzzer

Introduction

The functioning principle is magnetic. The diaphragm of the buzzer is made of magnetic material and it is located in a magnetic field created by a permanent magnet. The winding is not attached to the diaphragm as is the case with the speaker. The winding is located in the magnetic circuit so that it can alter the magnetic field of the permanent magnet, thus changing the magnetic force affecting the diaphragm.

The useful frequency range is approximately 2 kHz to 5 kHz.

Battery

Phone Battery

Introduction

The battery for the 6360 is the BLB-3 (Li-Ion 1000 mAh).

Interface

The battery block contains NTC and BSI resistors for temperature measurement and battery identification. The BSI fixed resistor value indicates the chemistry and default capacity of a battery. NTC-resistor measures the battery temperature. Temperature and

capacity information is needed for charge control. These resistors are connected to BSI and BTEMP pins of the battery connector. Phone has pull-up resistors (R202) for these lines so that they can be read by A/D inputs in the phone (see figure below). There also are spark gaps in the BSI and BTEMP lines to prevent ESD.

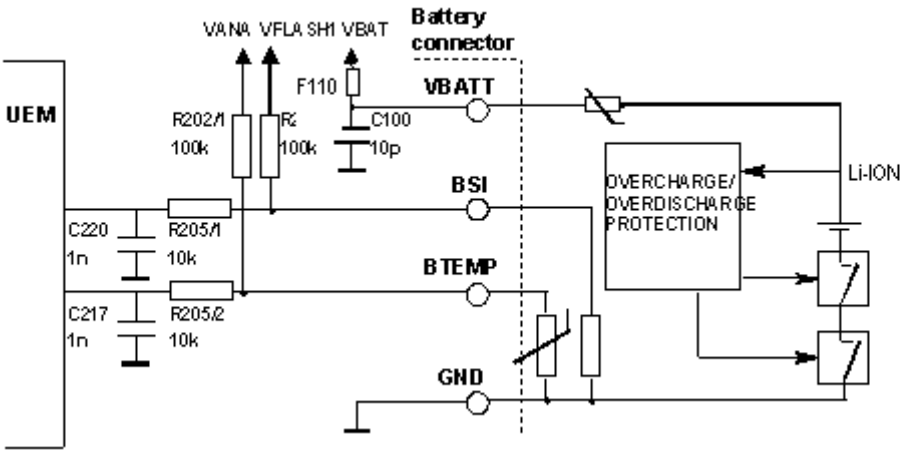

Figure 3: Battery Connections.

Batteries have a specific red line which indicates if the battery has been subjected to excess humidity. The batteries are delivered in a "protection" mode, which gives longer storage time. The voltage seen in the outer terminals is zero (or floating), and the battery is activated by connecting the charger. Battery has internal protection for overvoltage and overcurrent.

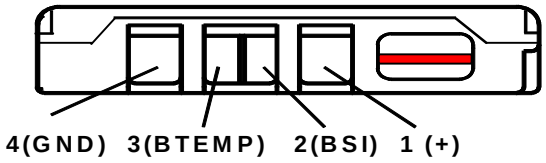

Figure 4: BLB-3 Battery contacts.

Battery Connector

The NPW-2NX battery connector (part of the system connector) is soldered to the board. This provides a more reliable, lower impedance connection.

#	Signal name	Connected from - to	UPP I/O	Signal properties A/D--levels--freq./timing Timing	Resolution	Description / Notes
MEMADDA(23:0) *		External Memory Address / Data Bus				
0-15	EXT AdDa 0.15	UPP	In/Out	I/O	25 / 150 ns	Burst Flash Address (0:15) Direct Mode Address (0:7)
16-23	EXTAd 16:23	UPP	Out	Out	25 / 150 ns	Burst Flash Address (16:23) Direct Mode Data (8:15)

Accessories Interface

System connector

Introduction

NPW-2NX uses DCT-3 accessories via a DCT-3 system connector.

Interface

The interface supports all DCT-3 accessories.

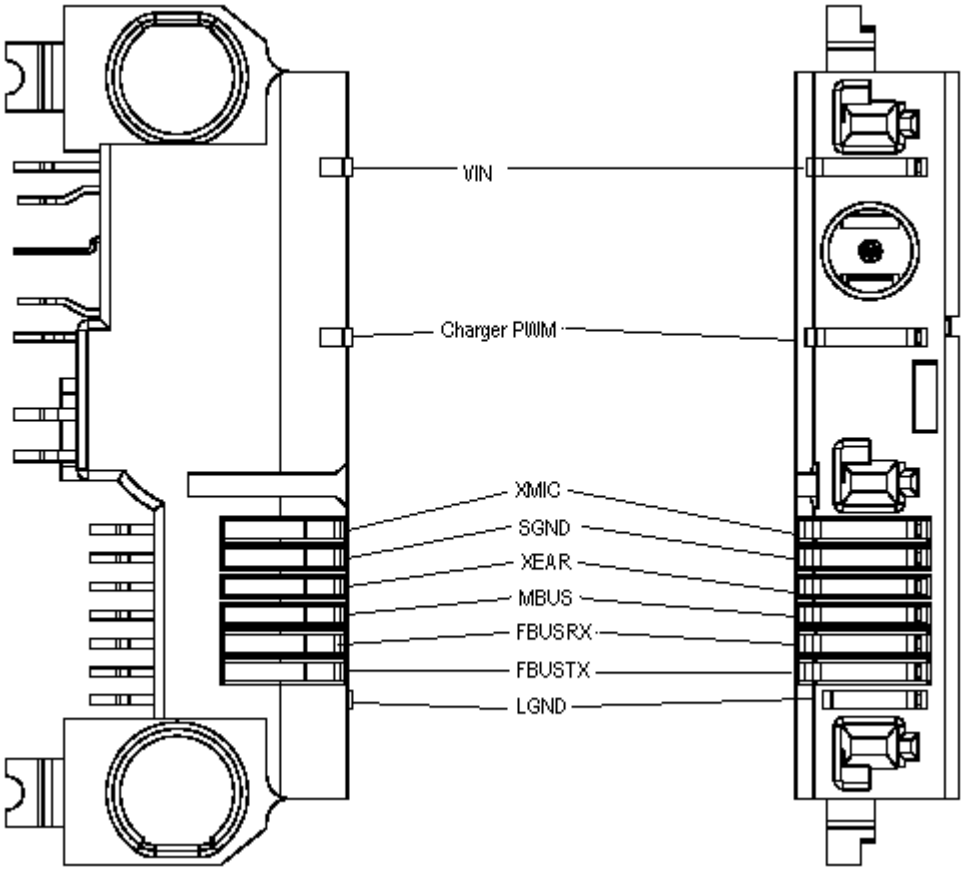

Figure 5: System Connector.

An accessory is detected by the HeadInt-line, which is connected to the XMIC. When the accessory is connected, it generates headint-interruption (UEMINT) to MCU. After that, hookInt line is used to determine which accessory is connected. This is done by the voltage divider, which consists of phone's internal pull-up and accessory specific pull-down. Voltage generated by this divider is then read by the ad-converter of UEM. The HookInt-interrupt is generated by the button in the headset or by the accessory external audio input.

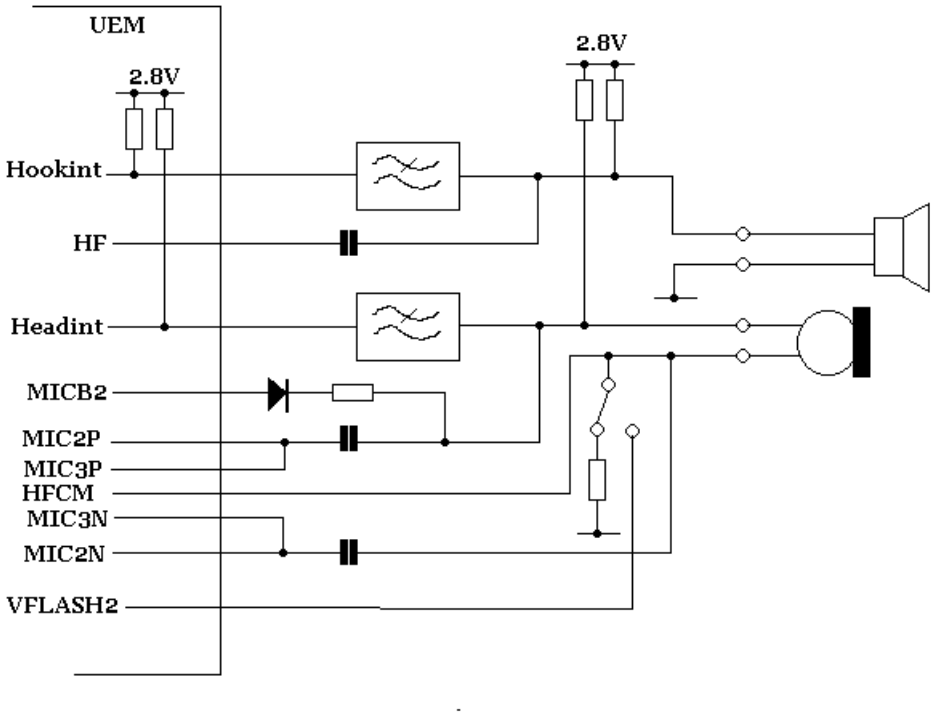

Figure 6: Accessory Detection / External Audio.

Technical Information

ESD protection is made by spark gaps, buried capacitor and inside UEM, which is protected ±8 kV. RF and BB noise is prevented by inductors.

IR module

Introduction

IR module is used for short-range data transfer. It is a low-power infrared transceiver module that is compliant with the IrDA 1.2 standard for fast infrared data communication. The IR module is located on top of the engine side, next to the Power switch.

Interface

IR transmit is controlled by TXD line coming from UPP.

The received infrared is detected and shaped by the module, and is sent straight to the UPP.

VFLASH1 is the power supply of the IR module except transmit. That is also filtered by capacitor (C350 and C352). The IR module is controlled by GENIO(10) from the UPP.

Technical Information

The IR interface is designed into the UEM. The IR link supports speeds from 9600 bit/s to 1.152 MBit/s, up to 1 m.

Charger IF

Introduction

The charger connection is implemented through the bottom connector. DCT-3 bottom connector supports charging with both plug chargers and desktop stand chargers.

The NPW-2NX supports 2-wire and 3-wire chargers. In the 2-wire configuration, charging is controlled by the UEM. In the 3-wire, a PWM (pulse width modulation) line controls charging.

Interface

The fuse F100 protects the phone from currents that are too high (for example, when broken or pirate chargers are used). L100 protects engine from RF noise, which may occur in charging cable. V100 also protects the UEM asic from reverse polarity charging voltage and from excessive charging voltage. C105 is also used for ESD and EMC protection. Spark gaps are used for ESD protection right after the charger plug.

Test Interfaces

Production Test Pattern

Interface for NPW-2NX production testing is 5-pin pad layout in BB area (see figure below). Production tester connects to these pads by using spring connectors. Interface includes MBUS, FBUSRX, FBUSTX, VPP and GND signals. Same pads also are used for AS test equipments such as module jig and service cable.

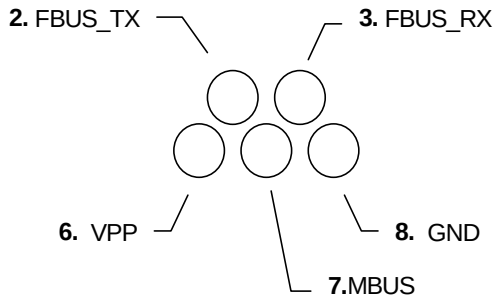

Figure 7: Top View of Production Test Pattern.

Other Test Points

Because BB asics and flash memory are CSP components, the access to BB signals is very poor. This makes measuring of most of the BB signals impossible. In order to debug BB at least on some level, the most important signals can be accessed from 0.6 mm test points. The figure below shows test points located between UEM and UPP.

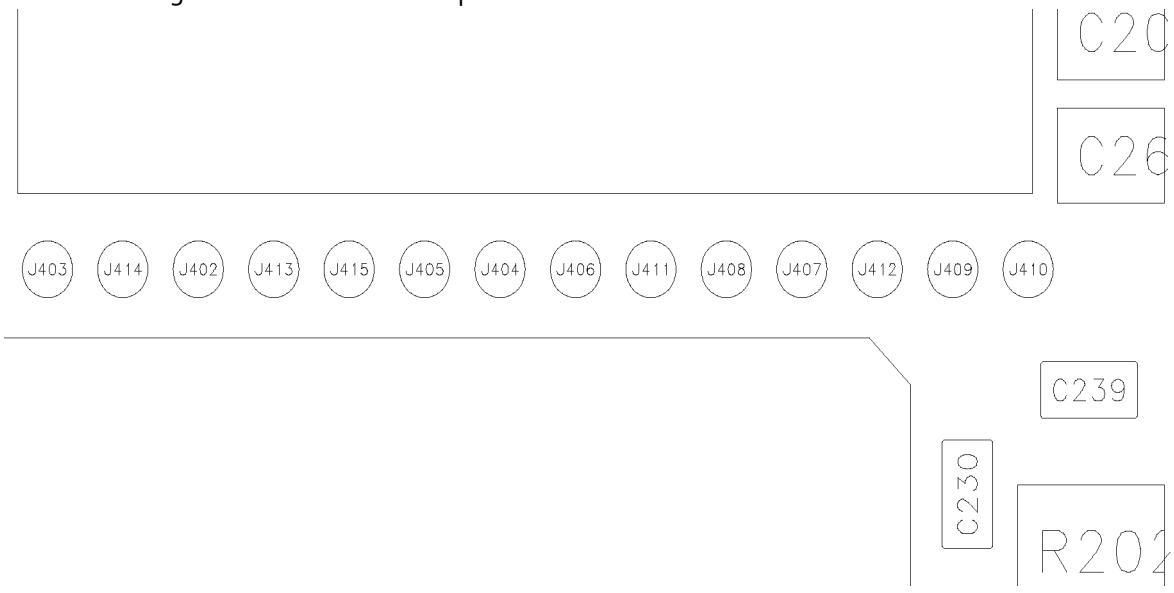

Figure 8: Test points Located Between UEM and UPP.

EMC

General

A protective metal deck is located underneath the battery. This deck is grounded to BB

shield as well as to the RF shield.

BB Component and Control IO Line Protection

Keyboard lines

The LN8 keyboard uses conventional row and column detection, with a conductive key dome shorting particular rows and columns together when pressed.

The keyboard is controlled entirely by the UPP. The rows and columns are ESD protected by diodes and spark gaps.

PWB

The top and bottom layers have gold flashed edges to reduce the risk of ESD damage through mechnical seams. Additionally, the lightguide outline is followed on the PCB with gold flash to divert ESD from sensitive electronics.

All holes in PWB are grounded and plated through holes (Note: LED holes cannot be grounded).

LCD

ESD protection for LCD is implemented by connecting metal frame of LCD in to gnd. Connection is only on one side, at the top of the LCD.

Microphone

The microphone's metal cover is connected to gnd and there are spark gaps on PWB. Microphone is an unsymmetrical circuit, which makes it well protected against EMC.

EARP

Earpiece is protected by spark gaps and 14 V varistors and low value resistors.

Buzzer

The buzzer is protected internal to the UEM, and externally by spark gaps.

IRDA

The IRDA is mechanically isolated from the outside of the phone, eliminating the need for extra protection.

System Connector Lines

	System Connector signals that have EMC protection						
Protection type	VIN	XMIXP	XMICN	XEARP	XEARN	HEADINT	MICP
ferrite bead (600 /199MHz)		X	X	X	X		X
ferrite bead (420 /100MHz)	X						
spark gaps		X	X	X	X	X	X
PWB capacitors		X	X	X	X	X	X
RC-circuit			X	X	X	X	X
capacitor to ground	X	X	X	X	X		

HF and HFCM lines have spark gaps, and a ferrite bead RF filter (450 W/100 MHz).

Headint and Hookint have spark gaps as well as an RC-circuit.

Charger + is protected with a ferrite bead (42 W/100 MHz) and a capacitor to ground (1 n).

Charger - is protected with a ferrite bead (42 W/100 MHz).

Battery Connector Lines

BSI and BTEMP lines are protected with spark gaps and RC-circuit where resistors are size 0603.

M-bus F-bus

The FBus and MBus lines are protected with ESD diodes, varistors, and RC filters.

Tranceiver Interfaces

BB - RF Interface Connections

All the signal descriptions and properties in the following tables are valid only for active signals.

RIP	Signal name	Connected from - to		BB I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
RFICCNTRL(2:0)				RF IC Control Bus from UPP to RF IC (SAFARI)				
0	RFBUSCLK	UPP	RFIC	In	Dig	0/1.8V (0: <0.4V 1: >1.4V	9.72 MHz	RF Control serial bus bit clock
1	RFBUSDA	UPP/ RFIC	RFIC UPP	I/O	Dig			Bi-directional RF Control serial bus data.
2	RFBUSEN1X	UPP	RFIC	In	Dig			RFIC Chip Set X

RIP	Signal name	Connected from - to		BB I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
PUL (2:0)				Power Up Reset from UEM to RF IC (SAFARI)				
0	PURX	UEM	RFIC	Out	Dig	0/1.8V	10us	Power Up Reset for RFIC
								SLCLK & SLEEPX not used in RF
GEN (28.0)				General I/= Bus connected to RF, see also separate collective GEN(28.0) table Control lines from UPP GENIOs to RF				
5	TXP1	RFIC, Lo-band mixer	UPP	Out	Dig	0/1.8V	10 us	Low Band Tx enabled
6	TXP2	RFIC	UPP	Out	Dig	0/1.8V		High band Tx enabled
RFCLK (not BUS -> no rip #)				System Clock from RF to BB, original source VCTCXO, buffered (and frequency shifted, WAM only) in RF IC (SAFARI)				
	RFCLK	VCTCXO -> RFIC	UPP	In	ANA	800mVpp typ (FET probed) Bias DC blocked at UPP input	19.44 MHz	System Clk from RF to BB
	RFClk GND	RF	UPP	In	Ana	0		System Clock slicer Ref GND, not separated from pwb GND layer
SLOWAD(6:0)				Slow Speed ADC Lines from RF block				
5	PDMID	RF Power detection module	UEM	In	Ana	0/2.7V dig	0/VR2	Power detection module identification to slow ADC (ch 5, previous VCTCXO Temp) signal to UEM
6	PATEMP	RF Power detection module	UEM	In	Ana	0.1-2.7V	-	Tx PA Temperature to UEM, NTC in Power Detection Module
RFCONV(9:0)				RF-BB differential Analog Signals: Tx I&Q, Rx I&Q and reference voltages				
0	RXIP	RFIC	UEM	In	Ana	1.4Vpp max. diff. 0.5Vpp typ bias 1.30V		Differential positive/negative in-phase Rx Signal
1	RXIN							
2	RXQP							Diff. positive/negative quadrature phase Rx Signal
3	RXQN							

RIP	Signal name	Connected from - to		BB I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
4	TXIP	UEM	RFIC	Out	Ana	2.2Vpp max. diff. 0.6Vpp typ bias 1.30V		Differential positive/negative in-phase Tx Signal
5	TXIN							
6	TXQP							Diff. positive/negative quadrature phase Tx Signal
7	TXQN							
9	VREFRFO1	UEM	RFIC	Out	Vref	1.35 V		RF IC Reference voltage from UEM
RFAUXCON(2:9)				**RF-BB Analog Control Signals to/from UEM**				
1	TXPWRDET	TXP Det.	UEM	In	Ana	0.1-2.4V	50 us	Tx PWR Detector Signal to UEM
2	AFC	UEM	VCTCXO	Out	Ana	0.1-2.4V		Automatic Frequency Control for VCTCXO
VRF Globals instead of Bus				**Regulated RF Supply Voltages from UEM to RF. Current values are of the regulator specifications, not the measured values of RF**				
	VR1 A	UEM	RFIC	Out	Vreg	4.75 V +- 3%	10mA max.	UEM, charge pump + linear regulator output. Supply for UHF synth phase det...
	VR1 B	UEM	RFIC	Out	Vreg	4.75 V +- 3%	10mA max.	UEM, charge pump + linear regulator output. Supply for Tx VHF VCO.
	VR2	UEM	RFDiscr./RFIC	Out	Vreg	2.78 V +- 3%	100 mA max.	UEM linear regulator. Supply voltage for Tx IQ filter and IQ to Tx IF mixer.
	VR3	UEM	VCTCXO	Out	Vreg	2.78 V +- 3%	20mA max.	UEM linear regulator. Power supply to VCTCXO + RFCLK Buffer in RF IC.
	VR4	UEM	RFIC	Out	Vreg	2.78 V +- 3%	50mA max.	UEM linear regulator. Power supply for LNA/RFIC Rx chain.
	VR5	UEM	RFIC	Out	Vreg	2.78 V +- 3%	50mA max.	UEM linear regulator. Power supply for RF low band PA driver section.
	VR6	UEM	RFIC	Out	Vreg	2.78 V +- 3%	50mA max.	UEM linear regulator. Power supply for RF high band PA driver section.
	VR7	UEM	RFIC, UHF VCO	Out	Vreg	2.78 V +- 3%	45mA	UEM linear regulator. Power supply for RF Synthes.
	IPA1	UEM	RF PA	Out	Iout	0-5 mA		Settable Bias current for RF PA L-Band
	IPA2	UEM	RF PA	Out	Iout	0-5 mA		Settable Bias current for RF PA H-Band
	VFLASH1	UEM	RFIC	Out	Iout	2.78V	12mA	UEM linear regulator common for BB. RFIC digital parts and F to BB digl. IF.

RIP	Signal name	Connected from - to		BB I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
VBATT, Global								
	VBATTRF	Batt Conn	RFPA	Out	Vbatt	3...5V	0...1A 2A peak	Raw Vbatt for RF PA

BB Internal Connections

UEM Block Signal Description

RIP	Signal name	Connected from - to		UEM I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
RFCONVDA(5:0)*				**1.8V digital interface between UPP and UEM. RF converter CLK. Rx and Tx I&Q data (bit stream signals).**				
0	RFCONVCLK	UPP	UEM	In	Dig	0/1.8V	4.86 MHz/ Digi 3.24 MHz / Ana	RF Converter Clock
1	RXID	UEM	UPP	Out				(PDM) RxI Data (PDM) RxQ Data
2	RXQD							
3	TXID	UPP	UEM	In				(PDM) TxI Data (PDM) TxQ Data
4	TXQD							
5	AUXDA	UPP	UEM	In				Auxiliary DAC Data
RFCONVCTRL(2:0)*				**1.8V digital interface between UPP (DSP) and UEM. RF converter UEM RF IF bidirectional serial Control Bus, "DBUS".**				
0	DBUSCLK	UPP	UEM	In	Dig	**0/1.8V**	9.72MHz	Clock for Fast Control to UEM
1	DBUSDA			In/ Out				Fast Control Data to/from UEM
2	DBUSENX			In				Fast Control Data Load / Enable to UEM
AUDUEMCTRL(3.0)*				**1.8V digital interface between UPP (MCU) and UEM. Bidirectional Control Bus "CBUS"**				
0	UEMINT	UEM	UPP	Out	Dig	0/1.8V		UEM Interrupt
1	CBUSCLK	UPP	UEM	In			1.08MHz	Clock for control/Audio Con-vertors in UEM
2	CBUSDA			In/ Out			1.08Mbit/ s	Control data
3	CBUSENX			In				Control Data Load Signal
AUDIODATA(1:0)*				**1.8V digital audio interface between UPP and UEM audio codec. PDM data clocked by CBUSCLK**				
0	EARDATA	UPP	UEM	In	Dig	0/1.8V	1.08Mbit/ s	PDM Data for Downlink Audio, clocked by CBUSCLK
1	MICDATA	UEM	UPP	Out				PDM Data forUplink Audio, clocked bu CBUSCLK
PUSL(2:0)*				**Power-Up & Sleep Control lines**				

RIP	Signal name	Connected from - to		UEM I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
0	PURX	UEM	UPP RFIC	Out	Dig	0/1.8V		Power Up Reset, 0 at reset
1	SLEEPX	UPP	UEM	In				Power Save Functions, 0 at sleep
2	SLEEPCLK	UEM	UPP	Out			32 KHz	32 KHz Sleep Clock
IACCDIF(5:0)*				**BB Internal 1.8V Digital Accessory Buses between UPP and 2.7V level shifter UEM**				
0 1	IRTX IRRX	UPP UEM	UEM UPP	Out In	Dig	0/1.8V	1.152 Mbit/s max	Infrared Transmit Infrared Receive
2 3	MBUSTX MBUSRX	UPP UEM	UEM UPP	In Out	Dig	0/1.8V	9k6 b/s 9k6 b/s < 7 Mb/s	MBUS Transmit MBUS Receive / FDL Clk
4 5	FBUSTXI FBUSRXI	UPP UEM	UEM UPP	In Out	Dig	0/1.8 V	<115kb/s <1Mb/s <115kb/s <7Mb/s	FBUS Transmit / FDL Tx FBUS Receive / FDL Rx

RIP	Signal name	Connected from - to		UEM I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
SLOWAD(6:0)*				**SLow Speed ADC Lines, UEM external**				
0	BSI	BAT-TERY	UEM	In	Ana	0-2.7V		Battery Size Indicator/FDL init
1	BTEMP							Battery Temperature
5	PDMid	RF PDMod	UEM	In	Ana	0-2.7V		Power detection module identification to slow ADC (ch, previous VCTCXO Temp) signal to UEM.
6	PATEMP	RF, PDMod NTC						
RFCONV(9:0)*				**RF - BB Analog Signals: Tx I&Q, Rx I&Q and ref**				
0	RXIP	RFIC	UEM	In	Ana	1.4Vpp max diff. 0.5Vpp typ bias 1.30V		Differential positive/negative in-phase Rx Signal
1	RXIN							
2	RXQP							Diff. positive/negative quadrature phase Rx Signal
3	RXQN							
4	TXIP	UEM	RFIC	Out	Ana	2.2Vpp max diff. 0.6VppTyp Bias 1.30V		Differential positive/negative in-phase Tx Signal
5	TXIN							
6	TXQP							Differential positive/negative quadrature phase Tx Signal
7	TXQN							

RIP	Signal name	Connected from - to		UEM I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
9	VREFRFO1	UEM	RFIC	Out	Vref	1.35V		RF IC Reference voltage from UEM
HP INTERNAL AUDIO								
AUDIO(4:0)			HP Internal analog ear & microphone IF between UEM and Mic/Ear circuitry					
0	EARP	UEM	Ear-piece	Out	Ana	1.25V	Audio	Differential signal to HP internal Earpiece. Load resistance 32 ohm.
1	EARN							
2	MIC1N	Mic	UEM	In	Ana	100mVpp max diff.	Audio	Differential signal from HP internal MIC, 2mV nominal
3	MIC1P							
4	MICB1	Mic	UEM	Out	V bias	2.1V typ./ <600 uA	DC Bias	Bias voltage for internal MIC
EXTERNAL AUDIO INTERFACE								
XAUDIO(9:0)*			External Audio IF between UEM and X-audio circuitry					
0	HEADINT	SysCon /HSet	UEM	In	Dig	0/2.7V		Input for Headset Connector HeadInt Switch
1	HF	UEM	SysCon /HSet	Out	Ana	1.0Vpp bias 0.8V	Audio	External Earpiece Audio Signal Reference output for DC coupled external Earpiece
2	HFCM				Ana	0.8 Vdc		
3	MICB2	UEM	SysCon /HSet	Out	V bias	2.1V typ/ 600 uA		Bias voltage for external MIC
4	MIC2P MIC2N	SysCon /Head-set	UEM	In	Ana	200mVpp max diff	Audio	Differential signal from external MIC
5								
6	HOOKINT	Sys Con	UEM	In	Ana/ Dig	0...2.7V	DC	HS Button interrupt, External Audio Accessory Detect (EAD)
CHARGER INTERFACE								
CHARGER lines, no bus*								
	VCHARGIN	Charge r	UEM	In	Vchr	< 16 V <1.2 V	DC	Vch from Charger Connector, max. 20 V
	GND				GND			GND from/to Charger connector
PWRONX *			Power On Signal, see also the UI/keyboard					
	PWRONX	UI	UEM	In	Dig	0/Vbatt		Power button
	GND				GND			GND from/to Charger connector
RFAUXCONV(2:0)			RF-BB auxiliary analog signals					
0								

RIP	Signal name	Connected from - to		UEM I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
1	TXPWRDET	TXPow. Det. Mod.	UEM	In	Ana	0.1-2.7V		Tx PWR Detector Output to UEM
2	AFC	UEM	VCTCXO	Out	Ana	0.1-2.4V	11bits	AFC control voltage to VCTCXO, default about 1.3V
IRIF, no bus no rips			UEM 2.7V signals to IR Module					
	IRLEDC	UEM	IR	Out	Dig	0/2.7V	9k6 - 1Mbit/s	IR Tx signal to IR Module
	IRRXN	IR	UEM	In	Dig	0/2.7V	9k6 - 1Mbit/s	IR Receiver signal from IR Module
UIDRV lines, no bus			UEM drivers: sinking outputs to Buzzer, Vibra, KLED, DLED					
	BUZZO	UEM	Buzzer	Out	Dig	350mA max. / Vbatt	1-5 kHz, PWM vol	Open collector sink switch output for Buzzer. Frequency controlled pitch, PWM for volume.
	VIBRA	UEM	Vibra	Out	Dig	135mA max / Vbatt	64/128/ 256/512 Hz	Open collector sink switch/Frequency/ pwm output for buzzer
	DLIGHT	UEM	UI	Out	Dig	100mA / Vbatt	Switch/ 100Hz pwm	Open drain switch/pwm output for display light
	KLIGHT	UEM	UI	Out	Dig	100mA / Vbatt	Switch/ 100Hz pwm	Open drain switch/pwm output for key light
ACCDIF lines, no bus *			Wired Digital Accessory Interface, only to test pattern					
	MBUS	UEM	Test Pad 7	In/ Out	Dig	0/2.7 V	9k6bit/s	Mbus bidirectional asynchronous serial data bus/FDL clock, 0-8MHz depends on project
	FBUSTXO	UEM	Test Pad 2	Out	Dig	0/2.7 V	9k6-115kbit/s	Fbus asynchronous serial data output / FDL data out <1Mbit/s
	FBUSRXO	Test Pad 3	UEM	In	Dig	0/2.7 V	9k6-115kbit/s	Fbus asynchronous serial data input/FDL in, 0-8Mbit/s depends on project
RTCBATT lines, no bus *			Connector pads for Real Time Clock back up battery					
	VBACK	UEM	RTC-BATT	In/ Out	Vsupply / Chrg	+2-3.3V		For back up battery Li 6.8x1.4 **2.3mAh@3.3V**
	GND	Global GND				0		
VBB, Globals instead of Bus*			Regulated BB Supply Voltages					
	VANA	UEM		Out	Vreg	2.78V +-3%	80mA max.	Disable in sleep mode
	VFLASH1	UEM		Out	Vreg	2.78V +-3%	70mA max	1.5mA max. in sleep mode. VFLASH1 is always enabled after power on.

RIP	Signal name	Connected from - to		UEM I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
	VFLASH2	UEM		Out	Vreg	2.78V +-3%	40mA max.	VFLASH2 is disabled by default
	VIO	UEM		Out	Vreg	1.8V +-4.5%	150mA max.	1.5mA max. in sleep mode. VIO is always enabled after power on.
	VCORE	UEM		Out	Vreg	1.0-1.8V +-5%	200mA max.	200 uA max. in sleep mode
	VBACK	UEM		In/ Out	Vreg	3.0 V		No external use, only for RTC battery charging/discharging.

UPP Block signals

RFCONVDA(5:0)	**See UEM / RFCONVDA(5:0)**
RFCONVCTRL(2:0)	**See UEM / RFCONVCONTR(2:0)**
AUDUEMCTRL(3:0)	**See UEM / AUDUEMCTRL(3:0)**
AUDIODATA(1:0)	**See UEM / AUDIODATA(1:0)**
ISIMIF(2:0)	**See UEM / ISIMIF(2:0)**
PUSL(2:0)	**See UEM / PUSL(2:0)**
IACCDIF(5:0)	**See UEM / IACCDIF(5:0)**

RFCLK & GND	**See BB_RF IF Conn / RFCLK (not BUS ...)**
RFICCNTRL(2:0)	**See BB_RF IF Conn / RFICCNTRL(2:0)**
GENIO(28:0)/rips 5 and 6	**See BB_RF IF Conn / GENIO(28:0) also Sec 5.2.4**

Rip #	Signal Name DAMPS/ GSM1900	Connected from --- to		UPP I/O		Signal Properties A/D--Levels---Freq./ Timing resolution		Description / Notes
UPP Globals, no bus, no rip				**Power supplies and GND**				
	VIO	UPP	UEM	In	Vreg	1.8 V +- 4.5 %	20mA max.	UPP I/O power supply
	VCORE	UPP	UEM	In	Vreg	1.0-1.8 V +- 5 %	100mA max.	UPP logics and processors power supply, settable to reach the speed for various clock frequencies.
	GND	UPP	VSSXXX			0		Global GND

MEMADDA(23:0)*	See Table 16. Memory Interface Signals / MEMADDA(23:0)*
MEMCONT(9:0)	See Table 16. Memory Interface Signals / MEMCONT(8:0)
GENIO(28:0)	See Table 16. Memory Interface Signals / GENIO(28:0)

RIP	Signal name	Connected from - to		UPP I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
GENIO(28:0)			**General I/O Pins. Bolded lines are only valid for one product**					
0	Switch control for SGND Vdd	UPP		Out	Dig	0-1.8 V	In/Pull Up	Used to enable/disable power to DLR-3 cable
1	Emu/Present	UPP		In	Dig	0-1.8 V	In/Pull Up	R&D only
2	RTS	UPP		In	Dig	0-1.8 V	In / Pull Up	Used as request to send input from DLR-3 cable
3	Not Used	UPP		Out	Dig	0-1.8 V	In / Pull Down	
4	**LCDRstX**	**UPP**	**Display**	Out	**Dig**	0-1.8 V	**Out / 0**	**Display reset**
5	**TXP1**	**UPP**	**RF**	Out	**Dig**	0-1.8 V	**Out / 0**	**Tx Power Enable (low Band)**
6	**TXP2**	**UPP**	**RF**	Out	**Dig**	0-1.8 V	**Out / 0**	**Tx Power Enable (High Band)**
7	Not Used	UPP		Out	Dig	0-1.8 V	In / Pull Down	
8	Not Used	UPP		Out	Dig	0-1.8 V	In / Pull Down	
9	Not Used	UPP		Out	Dig	0-1.8 V	In / Pull Down	
10	**IRModSD**	**UPP**	**IR Module**	Out	**Dig**	0-1.8 V	**In / Pull Down**	**IR Module Shut Down**
11	Bandset	UPP	RF / FMR	Out	Dig	0-1.8 V	In / Pull Up	Lo/Hi Band Selection (DAMPS) / Extended Band Selection (PDC)
12	AData	UPP		In/ Out	Dig	0-1.8 V	In / Pull Down	
13	Not Used	UPP	IR / RF	Out	Dig	0-1.8 V	In / Pull Up	Fast IR
14	Not Used	UPP		In	Dig	0-1.8 V	In / Pull Down	
15	Not Used	UPP		Out	Dig	0-1.8 V	In / Pull Down	
16	Not Used	UPP		In	Dig	0-1.8 V	In / Pull Up	
17	Not Used	UPP		In	Dig	0-1.8 V	In / Pull Up	
18	Not Used	UPP		Out	Dig	0-1.8 V	In / Pull Down	
19	Not Used	UPP	LPRF/ RF	In/ Out	Dig	0-1.8 V	In / Pull Down	LPFR Data In / Accessory Buffer Enable / PAGain
20	Not Used	UPP	LPRF	Out	Dig	0-1.8 V	Out / 0	LPRF Data Out

RIP	Signal name	Connected from - to		UPP I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
21	Not Used	UPP	LPRF	Out	Dig	0-1.8 V	In / Pull Up	LPRF Sync / Accessory Mute
22	Not Used	UPP	LPRF	Out	Dig	0-1.8 V	In / Pull Down	LPRF Interrupt/Accessory Power Up
23	**FLSWRPX**	**UPP**	**FLASH**	Out	**Dig**	0-1.8 V	**Out / 1**	**Write Protect, 0-active when protected**
24	Not Used	UPP		Out	Dig	0-1.8 V	In / Pull Up	
25	Not Used	UPP		In/ Out	Dig	0-1.8 V	In / Pull Up	
26	Not Used	UPP		Out	Dig	0-1.8 V	In / Pull Down	
27	Not Used	UPP		In/ Out	Dig	0-1.8 V	In / Pull Up	
28	Not Used	UPP		Out	Dig	0-1.8 V	Out / 1	

RIP	Signal name	Connected from - to		UPP I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
KEYB(10:0)*				**Keyboard matrix**				
0	P00	UPP	KEY-BOARD	In	Dig	0-1.8 V		Keyboard Matrix Line S0. Not used.
1	**P01**	**UPP**	**KEY-BOARD**	**In**	**Dig**	**0-1.8 V**		Keyboard Matrix Line S1
2	**P02**							Keyboard Matrix Line S2
3	**P03**							Keyboard Matrix Line S3
4	**P04**							Keyboard Matrix Line S4
5	**P010**	**UPP**	**KEY-BOARD**	**In**	**Dig**	**0-1.8 V**		Keyboard Matrix Line R0
6	**P011**							Keyboard Matrix Line R1
7	**P012**							Keyboard Matrix Line R2
8	**P013**							Keyboard Matrix Line R3
9	**P014**							Keyboard Matrix Line R4
10	P015	UPP	KEY-BOARD	In	Dig	0-1.8 V		Keyboard Matrix Line R5. Not used.
LCDUI lines, no bus *			**Display & UI Serial Interface**					

RIP	Signal name	Connected from - to		UPP I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
	LCDCamClk	UPP	DIS-PLAY	Out	Dig	0-1.8 V	4.86 MHz/ 2.43 MHz	Data clock for LCD serial bus, the speed may vary according to the display and direction requirements.
	LCDCamTxDa			I/ Out	Dig		4.86 MHz/ 2.43 Mbit/s	Serial Data to/from LCD
	LCDCSX			Out	Dig			LCD Chip Select
	GENIO(4)			Out	Dig			LCD Reset, 0-active

MEMORY Block Interfaces

RIP	Signal name	Connected from - to		I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
MEMADDA(23:0)*			External Memory Access / Data Bus					
0-15	EXTADDA 0:15	Mem-ory	UPP	In/ Out	Dig	0/1.8V	25 / 150 ns	Burst Flash Address (0:15) & Data (0:15) Direct Mode Address (0:7)
16-23	EXTAD 16:23	Mem-ory	UPP	In	Dig	0/1.8V	25 / 150 ns	Burst Flash Address (16:23) Direct mode Data (8:15)
MEMCONT(9:0)			External Memory Control Bus					
0	ExtWrX	Memor y_WE	UPP	In	Dig	0-1.8V		Write Strobe
1	ExtRdX	Memor y_OE	UPP	In				Read Strobe
2								
3	(FlsBAAX) VPPCTRL	Mem-ory (VPP)	UPP	In				VPP = 1.8V, => VIO used internally for VPP VPP = 5/12V, VPP used
4	FlsPS	Mem-ory PS	UPP	In/ Out			25 ns	Burst Mode Flash Data Invert Direct Mode Address (17)
5	FlsAVDX	Memor y_AVD	UPP	In				Flash Addr Data Valid/ Latch Burst Addr Direct Mode Address (18)
6	FlsCLK	Mem-nory CLK	UPP	In			50 MHz	Burst Mode Flash Clock Direct Mode Address (19)
7	FlsCSX	Memor y_CE	UPP	In				Flash Chip Select
8	FlsRDY	Mem-ory RDY	UPP	Out				Ready Signal for Flash
9	FlsRSTX	Memor y_RP	UPP	Out				Flash reset, 0 active (FLSRPX)
GENIO(28:0)			General I/O Pin used for extra control					
23	FLSWRPX	Memor y_WP	UPP	Out	Dig	0/1.8V	0	Write Protect, 0-active protected.
Globals			Power supplies and production test pad					
	VIO	UEM	FLASH	In	PWR	1.8V		FLASH power supply
	VPP	Prod TP 6	FLASH	In	Vpp	0/(1.8) /5/12V		FLASH programming/erasing voltage control. 5 or 12 external voltage for high speed programming
	GND							Global GND

Rip #	Signal Name DAMPS/ GSM1900	Connected from-- to		I/O		Signal Properties A/D--Levels---Freq./ Timing resolution		Description / Notes
MEMADDA(23:0)				**External Memory Addr/Data Bus**				
0-15	EXTADDA 0:15	Memory	UPP	In/Ou	Dig	0/1.8 V	25 / 150 ns	Burst Flash Address (0:15) & Data (0:15) Direct Mode Address (0:7)
16-23	EXTAD 16:23	Memory	UPP	In	Dig	0/1.8 V	25 / 150 ns	Burst Flash Address (16:23) Direct Mode Data (8:15)
MEMCONT(8:0)				**External Memory Control Bus**				
0	ExtWrX	Memory _WE	UPP	In	Dig	0/1.8 V		Write Strobe
1	ExtRdX	Memory _OE	UPP	In				Read Strobe
2								
3	(FlsBAAX) VPPCTRL	Memory (VPP)	UPP	In				VPP=1.8V ,=> VIO used internally for VPP VPP=5/12V, VPP used
4	FlsPS	Memory PS	UPP	In/ Out			25 ns	Burst Mode Flash Data Invert Direct Mode Address (17)
5	FlsAVDX	Memory _AVD	UPP	In				Flash Addr Data Valid/ Latch Burst Addr Direct Mode Address (18)
6	FlsCLK	Memory CLK	UPP	In			50 MHz	Burst Mode Flash Clock Direct Mode Address (19)
7	FlsCSX	Memory _CE	UPP	In				Flash Chip Select
8	FlsRDY	Memory RDY	UPP	Out				Ready Signal for Flash
9	FlsRSTX	Memory _RP	UPP	Out				Flash reset, 0 active, (FLSRPX)
GENIO(28:0)				**General I/O Pin used for extra control**				
23	FLSWRPX	Memory _WP	UPP	Out	Dig	0/1.8 V	O	Write Protect, 0-active protected
Globals				**Power supplies and production test pad**				
	VIO	UEM	FLASH	In	PWR	1.8 V		FLASH power supply
	VPP	Prod TP 6	FLASH	In	Vpp	0/(1.8) /5/12V		FLASH Programming/erasing voltage/control. 5 or 12 V external voltage for high speed programming
	GND							Global GND

IR Block Interfacesl

RIP	Signal name	Connected from - to		IR-Module I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
IRIF, no bus, no rips *				Module IR Interface				
	IACCDIF(0)	UPP	IR	In	Dig	0/1.8V	9k6 - 1Mbit/s	IR Tx signal to IR Module

RIP	Signal name	Connected from - to		IR-Module I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
	ICCADIF(1)	UPP	IR	Out	Dig	0/1.8V	9k6 - 1Mbit/s	IR Receiver signal from IR Module
GENIO(28:0)				**General I/O Bus**				
10	GENIO10	UPP	IR	In	Dig	0/1.8V		IR Module Shutdown, discrete inverting level shifter to 2.7V
Globals								
	VBAT	Battery	IR	In	Vbat	3.6V	1 = 500mA peak @Tx	Transmitter IR LED power supply from battery 3.6V nominal, 3...5.1V total range
	VFLASH1	UEM	IR	In	Vreg	2.78V +- 3%	1=99uA max. @Rx	IR Receiver and Transmitter power supply
	GND							
	VIO	UEM	IR	In		1.8V		Used to supply IR module interface logic

Audio Interfaces

RIP	Signal name	Connected from - to	AUDIO I/O			Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
HP INTERNAL AUDIO								
AUDIO(4:0)			HP Internal microphone and earpiece IF between UEM and Mic/Ear circuity					
0	EARP	UEM	Ear-piece	Out	Ana	1.25V	Audio	Differential signal to HP internal Earpiece. Load resistance 32 ohm.
1	EARN							
2	MIC1N	Mic	UEM	In	Ana	100mVpp max diff.	Audio, AC coupled to UEM	Differential signal from HP internal MIC
3	MIC1P							
4	MICB1	Mic	UEM	Out	V bias	2.1V typ./ <600 uA		Bias voltage for internal MIC
System Connector			HP Internal microphone IF between System Connector and Mic/ear circuitry					
	MIC+	Mic	Audio - UEM	In Out	Ana Bias	2mV nom 2V2kohm	Audio DC bias	Mic bias and audio signal. Microphone mounted into system connector
	MIC			In	GND	0 (GND)		AGND coupled to GND at UEM
Earpiece Connector Pads			HP Internal IF between Earpiece and Mic/Ear circuitry					
	"1"-EARP	EAR	Audio - UEM-EAR P/N	Out	Ana	1.25V	Diff DC coupled Audio	Differential audio signal to earpiece 32 ohm

RIP	Signal name	Connected from - to	AUDIO I/O			Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
EXTERNAL AUDIO INTERFACE								
XAUDIO(9:0)*			External Audio IF between UEM and X-audio circuitry					
0	HEADINT	SysCon /HSet	UEM	Out	Dig	0/2.7V		Output to UEM for Headset Connector "HeadInt" Switch
1	HF	UEM	SysCon /HSet	In	Ana	1.0Vpp bias 0.8V	Audio	ExternalEarpiece Audio Signal Reference for DC coupled external Earpiece
2	HFCM				Ana	0.8 Vdc		
3	MICB2	UEM	SysCon /HSet	Out	V bias	2.1V tvp/ 600 uA		Bias voltage for external MIC
4	MIC2P MIC2N	SysCon /Head-Set	UEM	Out	Ana	200mVpp max diff	Audio	Differential signal from external MIC
5								

RIP	Signal name	Connected from - to		AUDIO I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
6	HOOKINT	Sys Con	UEM	Out	Ana/ Dig	0...2.7 V	DC	HS Button interrupt, External Audio Accessory Detect (EAD)
7								Not used
8								Not used
9								Not used
System Connector			**HP Internal microphone IF between system connector and Mic/Ear circuitry**					
	XMICP	HS/HF Mic	**Audio - UEM**	In Out	Ana Bias	2/60mV nom diff 2.1V bias 1kohm	Audio DC bias	Headset Mic bias and audio signal 2mV nominal. HF Mic signal 60mV nominal. Differential symmetric input. Accessory detection by bias loading (EAD channel of slow ADC of UEM) Hook interrupt by heavy bias loading Mic - connecting to GND through lower part of split symmetric load resistor (2 x 1 kohm) SGND can be used as a pseudo differential input with XMIC, and also as a DC power output for DLR-3 data cable.
	SGND			In	Ana	330Ohm to LGND or 2.8Vdc supply	Audio	
	XEARP	HS/HF EAR/ Amp.	Audio - UEM	In	Ana	100 mV nom diff	Audio	Quasi differential DC-coupled earpiece/HF amplifier signal to accessory. DC biased to 0.8V; XEARN a quiet reference although have signal when loaded due to internal series resistor.
	XEARN							

Key/Display blocks

RIP	Signal name	Connected from - to	KEY I/O			Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
KEYB(10:0)			Keyboard matrix, Roller key					
0	P00	Not used	UPP	Out	Dig	0/1.8V		
1	P01	Keyboard						Keyboard Matrix Line
2	P02	Keyboard						Keyboard Matrix Line
3	P03	Keyboard						Keyboard Matrix Line
4	P04	Keyboard						Keyboard Matrix Line
5	P10	Keyboard						Keyboard Matrix Line
6	P11	Keyboard						Keyboard Matrix Line
7	P12	Keyboard						Keyboard Matrix Line
8	P13	Keyboard						Keyboard Matrix Line
9	P14	Keyboard						Keyboard Matrix Line
10	P15	Not Used						
PWR_KEY			Power Key, not a member of the keyboard matrix					
	PWR_KEY	Power key	UEM	Out	Dig	0/Vbatt		Power key, not a member of the keyboard matrix

RIP	Signal name	Connected from - to	Display I/O			Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
LCDUI(2:0)			Display & UI Serial Interface					
0	LCDCAMCLK	UPP	Displ	In	Dig	0/1.8V	1 MHz	Clock to LCD
1	LCDCAMTXD	UPP	Displ	In/ Out	Dig	0/1.8V	1 MHz	Data to/from LCD
2	LCDCSX	UPP	Displ	In	Dig	0/1.8V		LCD Chip Select
GENIO(28:0)			General I/O Pins					
4	LCDRstX	UPP	Displ	Out	Dig	0/1.8V	Out / 0	Display Reset, 0-active

Baseband External Connections

RIP	Signal name	Connected from - to		Sys Conn I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
System Connector			HP Internal microphone IF between System Connector and Mic/Ear circuitry					
	XMICP	HS/HF Mic	Audio - UEM	In Out	Ana Bias	2/60mV nom diff 2V2koh m	Audio DC bias	Headset Mic bias and audio signal 2mV nominal. Hf Mic signal 60mV nominal. Differential symmetric output. Accessory detection by bias loadind. Hook interrupt by heavy bias loading. SGND can be used as a pseudo differential input with XMIC, and also as a DC power outlet for DLR-3 data cable.
	SGND			In	Ana	3300hm to LGND or 2.8Vdc supply	Audio	
	XEARP	HS/HF EAR/ Amp.	Audio-UEM	In	Ana	100mV nom diff	Audio	Quasi differential DC-coupled earpiece/HF amplifier signal to accessory. DC biased to 0.8V; XEARN a quiet reference although have signal when loaded due to internal series resistor.
	XEARN							
	INT	Switch	Audio - UEM	In	Dig	0/2.7V		HS interrupt from system connector switch when plug inserted
CHARGER INTERFACE								
CHARGER lines, no bus *								
	VCHARIN	Charger	UEM	In	Vchr	< 16V <1.2A	DC	Vch from Charger Connector, max 20V
	GND				GND			GND from/to Charger connector
	CHRGCTRL	Input	Output			32Hz, 0/2.8V		PWM control line for 3-wire chargers

RIP	Signal name	Connected from - to		Batt Conn I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
	GND	Globally	Batt -					Global GND
	VBAT		Batt +		Vbatt	3.0-4.2V	DC	Battery Voltage
	BSI		UEM		Ana Ana	0-2.7V	Pull down res	Battery Size Indicator Resistor, 100 kohm pull up to 2.78V(VFLASH)
	BTEMP		UEM					Btemp NTC Resistor, 100 kohm pull up to 2.78V(VANA)

Test Pattern for Production Tests

RIP	Signal name	Connected from - to		UI I/O		Signal Properties A/D Levels-Freq./ Timing resolution		Description / Notes
2	FBUSTX / FDLTX	Test Point	UEM	Out	Dig	0/2.7V		Fbus asynchronous serial data output / FDL
3	FBUSRX / FDLRX	Test Point	UEM	In	Dig	0/2.7V		Fbus asynchronous serial data input / FDL RxData
6	VPP	Test Point	Mem-ory	Out	Ana	0/5/12V		External Flash Programming Voltage for Flash Memory
7	MBUS / FDL-CLK	Test Point	UEM	In/ Out	Dig	0/2.7V	9k6bit/s	Mbus bidirectional asynchro-nous serial data bus/FDL Clock
8	GND	Test Point	BB					Ground

General Information About Testing

Phone operating modes

Phone has three different modes for testing/repair. Modes may be selected with suitable resistors connected to BSI- and BTEMP- lines as follows:

Mode	BSI- resistor	BTEMP- resistor	Remarks
Normal	68 k	47 k	
Local	560_ (<1k_)	whatever	
Test	> 1 k	560_(<1k_)	Recommended with baseband testing. Same as local mode, but it is possible to make a phone call.

The MCU software enters automatically to local or test mode at start-up if correspond ing resistors are connected.

Note! Baseband doesn't wake up automatically when the battery voltage is connected (normal mode). Power can be switched on by

- Pressing the power key
- Connecting a charger
- RC-alarm function

In the local and test mode, the baseband can be controlled through MBUS or FBUS (FBUS is recommended) connections by Phoenix service software.

RF Module

Requirements

The NPW-2 RF module supports the following systems:

AMPS

TDMA800

TDMA1900

Hence, the minimum transceiver performance requirements are described in TIA/EIA-136-270. The NPW-2NX RF must follow the requirements in revision A. EMC requirements are set by FCC 47CFR 15.107 (conducted emissions), 15.109 (radiated emissions, idle mode), and 22.917 (radiated emissions, call mode) [1].

The dualband RF-module is capable of seamless operation between 800 MHz and 1900 MHz bands with measuring capability for cross-band hand-offs and maho-measurements.

Temperature Conditions

Temperature range:

ambient temperature: -30...+ 60 °C

PWB temperature: -30...+85 °C

storage temperature range: -40 to + 85 °C

All of the EIA/TIA-136-270A requirements are not exactly specified over temperature range. For example, RX sensitivity requirement is 3 dB lower over –30..+60 °C range.

Main Technical Characteristics

RF Frequency Plan

The NPW-2NX frequency plan is shown in the following figure. A 19.44 MHz VCTCXO is used for UHF and VHF PLLs and as a baseband clock signal. All RF locals are generated in PLLs.

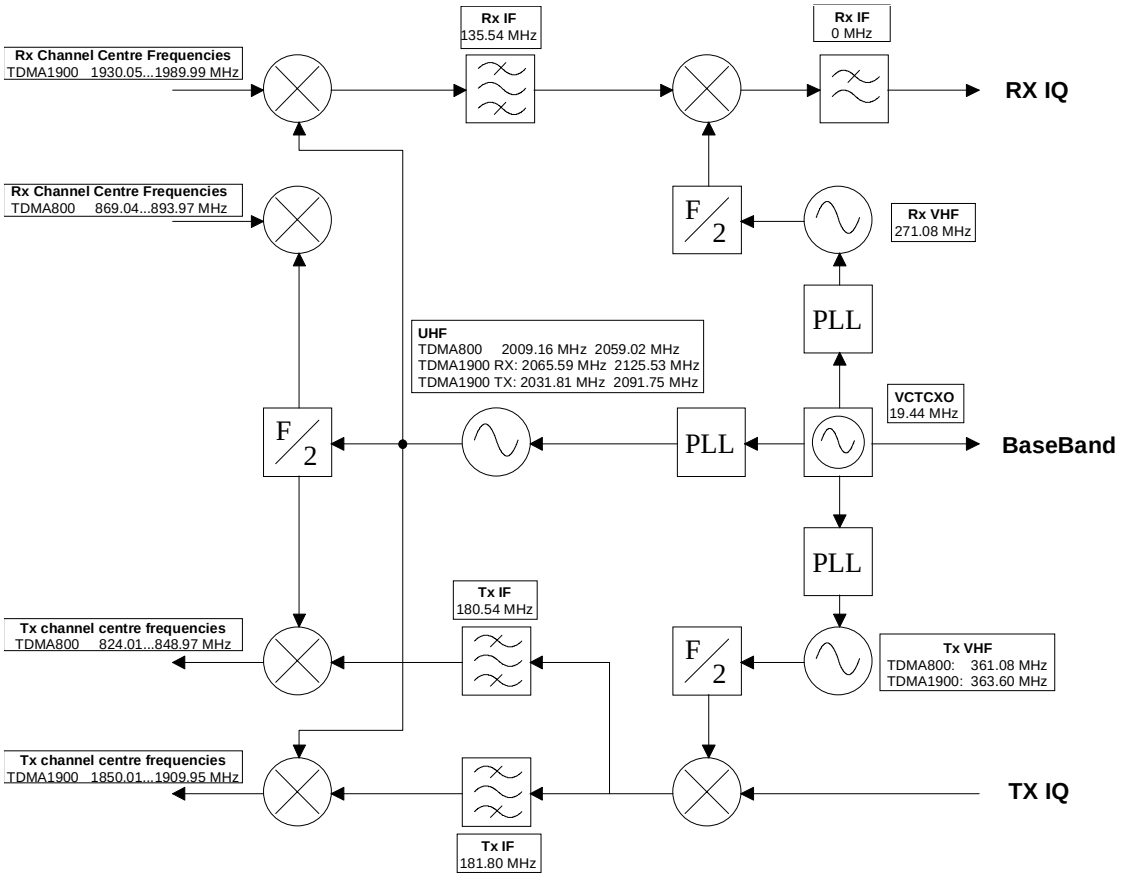

Figure 9: RF Frequency Block Plan.

The RX intermediate frequency is the same on both operating bands. Due to the AMPS mode simultaneous reception and transmission, TX and RX IF frequencies are exactly 45 MHz apart from each other. RXIF is 135.54 MHz and TXIF 180.54MHz. The RXIF frequency is set so that it is not a multiple of either of the VHF's comparison frequency (120 k). The digital-only operation on highband allows a free selection of the TX IF frequency, since separate TXIF filters are implemented. Hence, the highband TX IF frequency is freely fixed to 181.8MHz due to the best possible spurious signal filtering. Therefore, the UHF frequency needs to be changed according to TX and RX slots in TDMA1900 operation.

DC Characteristics

Power Distribution Diagram

Note: The current values in the figure below are not absolute values and cannot be measured. These values represent maximum/typical currents drawn by the corresponding RF or SAFARI blocks in use, and are, therefore, dependent on the phone's operating mode and state.

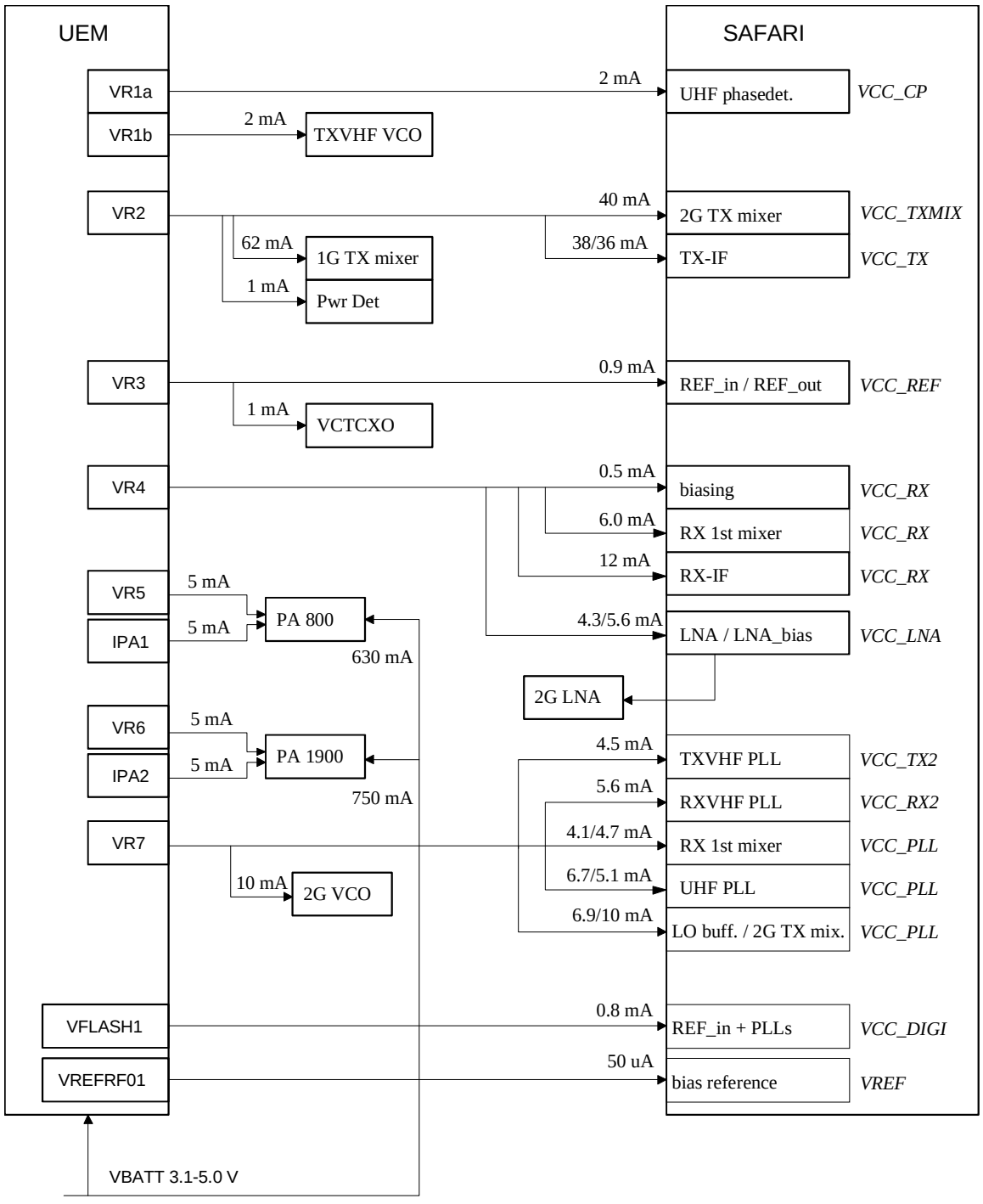

Figure 10: NPW-2NX Frequency Plan.

Regulators

The regulator circuit is the UEM and the specifications can be found in the table below:

Regulator name	Output voltage (V)	Regulator Max. current (mA)	RF total 1GHz	RF total 2GHz
VR1 a/b	4.75 ± 3%	10	4	4
VR2	2.78 ± 3%	100	100	76
VR3	2.78 ± 3%	20	2	2
VR4	2.78 ± 3%	50	23	24
VR5	2.78 ± 3%	50	5	5
VR6	2.78 ± 3%	50	5	5
VR7	2.78 ± 3%	45	40	45
IPA1, IPA2	2.7 max.	1 ± 10% 3 ± 4% 3.5 ± 4% 5 ± 3%	1.3 – 5.0	1.3 – 3.7
VREFRF01	1.35 ± 0.5%	0.12	0.05	0.05
VFLASH1	2.78 ± 3%	70	1	1

Receiver

The receiver shows a superheterodyne structure with zero 2nd IF. Lowband and highband receivers have separate frontends from the diplexer to the first IF. Most of the receiver functions are integrated in the RF ASIC. The only functions out of the chip are highband LNA, duplexers, and SAW filters. In spite of a slightly different component selection, the receiver characteristics are very similar on both bands.

An active 1st downconverter sets naturally high gain requirements for preceding stages. Hence, losses in very selective frontend filters are minimized down to the limits set by filter technologies used and component sizes. LNA gain is set up to 16dB, which is close to the maximum available stable gain from a single stage amplifier. LNAs are not exactly noise matched in order to keep passband gain ripple in minimum. Filters have relative tight stopband requirements, which are not all set by the system requirements but the interference free operation in the field. In this receiver structure, linearity lies heavily on mixer design. The 2nd order distortion requirements of the mixer are set by the 'half IF' suppression. A fully balanced mixer topology is required. Additionally, the receiver 3rd order IIP tends to depend on active mixer IIP3 linearity due to pretty high LNA gain.

The IF stages include a narrowband SAW filter on the 1st IF and a integrated lowpass filtering on zero IF. The SAW filter guarantees 14dBc attenuation at alternating channels, which gives acceptable receiver IMD performance with only moderate VHF local phase noise performance. The local signal's partition to receiver selectivity and IMD depends then mainly on the spectral purity of the 1st local. Zero 2nd IF stages include most of the receivers signal gain, AGC control range, and channel filtering.

AMPS/TDMA 800 MHz Front End

Parameter	MIN	TYP	MAX	Unit/Notes
Diplexer input loss	0.35	0.4	0.45	dB
Duplexer input loss	2.5	3	4.1	dB
LNA gain: High gain mode Low gain mode	16 -4.5	16.5 -4	17.3 -3.8	dB dB
LNA noise figure*	1.4	1.7	2.3	dB
LNA 3rd order intercept (IIP3)*	-4	-3	-1.5	dBm
Bandfilter input loss	1.5	2	2.5	dB
Mixer gain*	6	7.5	8	dB
Mixer NF*	8	9	10.5	dB
Mixer IIP3*	4	4.5	5	dBm
Total:				
Gain	18.2	18.6	20	dB
Noise Figure	4.6	5.5	7	dB
3rd order intercept (IIP3)	-8.9	-7.5	-6.8	dBm
*see Safari spec/measurements				

TDMA 1900 MHz Front End

The TDMA 1900 LNA is a discrete circuit. It uses an integrated Bias control block, which is inside the SAFARI. In normal high-gain operation mode, the bias voltage 2.78 V is connected on collector and sink type constant current source is connected on emitter. Bias current source is adjustable from 0.5 mA to 7.5 mA with 0.5 mA step. Base is biased from 2.78 V voltage via resistor.

When the LNA AGC step is enabled, LNA is in low gain operation mode. Voltage and current bias sources and direction of current are switched on the contrary. In this operation mode, the LNA has good linearity, a low noise figure, and about -3 dB gain.

During the TX-slot, LNA is in power-down mode. This is executed by switching the bias current source to 0 mA.

Parameter	MIN	TYP	MAX	Unit/Notes
Diplexer input loss	0.45	0.5	0.55	dB
Duplexer input loss	1.3	2.5	3.0	dB
LNA gain: High gain mode Low gain mode	14 -3.5	15 -3.0	15.5 -2.0	dB dB
LNA noise figure*	1.0	1.2	1.5	dB
LNA 3rd order intercept (IIP3)*	-3	-2	-1	dBm

Parameter	MIN	TYP	MAX	Unit/Notes
Bandfilter input loss		3.6	4.5	dB
Mixer gain*	6.5	7.5	8.5	dB
Mixer NF*	9	10	11	dB
Mixer IIP3*	4	4.5	5	dBm
Total:				
Gain	16.0	17.0	18.0	dB
Noise Figure	5.0	5.5	6.5	dB
3rd order intercept (IIP3)	4	5	6	dB
*see Safari spec/measurements		-70	-68	dBc

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Total				
Power up time			0.1	ms
Noise figure, total			9.5	dB
3rd order input intercept point		-25		dBm
Max voltage gain, Mixer + 2nd IF (IF+2nd AGC max)	78.5			dB
Min voltage gain, Mixer + 2nd IF (IF+2nd AGC min.)			6	dB
Gain charge, Mixer+2nd IF		1.4	0.9	dB, temp -30...+85 C
IQ mixers + AMP2				
RF input impedance differential		1.2		kohm/pF
RF input frequency range		135.54		MHz
Conversion gain @ Rl=1kohm	23.5	24	24.5	dB
IF AGC gain range (5x6 dB)	30			dB
IF AGC gain step (5 steps)		6		dB
IF AGC gain error relative to max gain	-0.5		+0.5	dB
AMP2 gain		18		dB
-3dB frequency	21	25	29	kHz
LPF: 4th order Chebysev				
LPF gain		0		dB
Corner frequency tuning range	14		17	kHz

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Corner frequency tuning step			1	kHz
Attentuation @ 30 kHz *	24			dB
Attentuation @ 60 kHz *	55			dB
Attentuation @ 120 kHz *	80			dB
Attentuation @ 240 kHz *	60			dB
Attentuation @ >480 kHz *	40			dB
AGC				
AGC gain range	-6		36**	dB
AGC gain range step 7 steps		6		dB
AGC gain error relative to max gain	-0.5		+0.5	dB
Max IF/2nd IF buffer output level			3	V pp (differential)

Frequency Synthesizers

NPW-2NX contains three synthesizers—one UHF synthesizer and two VHF synthesizers. The UHF synthesizer is based on an integrated PLL and external UHF VCO, loop filter, and VCTCXO. Its main goal is to achieve the channel selection for dual band operations associated with dual mode. Due to the RX and TX architecture, this UHF synthesizer is used for down conversion of the received signal and for final up conversion in transmitter. A common 2GHz UHFVCO module is used for operation on both low and highband. A frequency divider is integrated in the Safari.

Two VHF synthesizers consist of: RX VHF Synthesizer includes integrated PLL and VCO and external loop filter and resonator. The output of RX-VHF PLL is used as LO signal for the second mixer in receiver. TX VHF Synthesizer includes integrated PLL and external amplifier, loop filter, and resonator. The output of TX-VHF PLL is used as a LO signal for the IQ-modulator of the transmitter.

Transmitter

The transmitter RF architecture is an up-conversion type (desired RF spectrum is low side injection) with (RF-) modulation and gain control at IF. The IF frequency is band related—180.54 MHz in the cellular band and 181.80MHz in the PCS band. The cellular band is from 824.01-848.97 MHz and the PCS band is from 1850.01-1909.95 MHz.

Common IF

The RF-modulator is integrated with a PGA (Programmable Gain Amplifier) and IF output buffer inside the SAFARI_T RFIC-chip (I- and Q-signals that are output signals from BB-side SW IQ-modulator have some filtering inside Safari before RF-modulation is performed). The required LO-signal from the TXVCO is buffered with phase sifting in Safari. After modulation ($\pi/4$ DQPSK or FM), the modulated IF signal is amplified in the PGA.

Cellular Band

When operating in cellular band, the IF signal is buffered at IF output stage that is enabled by TXP1 TX control. The maximum linear (balanced) IF signal level to 50Ω load is about –8 dBm.

For proper AMPS-mode receiver (duplex) sensitivity, IF signal is filtered in strip-filter before up-conversion. The upconverter mixer is actually a mixer with LO and output driver being able to deliver about +6 dBm linear output power. Note that in this point, term linear means –33 dB ACP. The required LO power is about –6 dBm. The LO signal is fed from Safari.

Prior to the power amplifier, the RF signal is filtered in a band-pass filter. The typical insertion loss is about –2.7 dB, and maximum less than –3.5 dB. The input and output return losses are approximately -10 dB.

The power amplifier is 50Ω/50Ω module. It does not have its own enable/disable control signal, but it can be enabled by bias voltage and reference bias current signals. The gain window is +27 to +31 dB and the linear output power is +30dBm (typical condition) with –28 dB ACP. The nominal efficiency is 50 percent.

PCS Band

During operation in the PCS band, the IF signal is routed from the Safari to be filtered in the TX IF SAW filter. The signal is returned to the Safari, and then routed to the up-converter mixer. The LO-signal to the mixer is buffered and balanced inside the Safari. The mixer output is enabled by the TXP2 TX control signal. The maximum linear (balanced) RF signal level to a 50Ω load is about +7 dBm.

After the Safari, the balanced RF-signal is single-ended in 1:1 balun and then filtered in SAW filter. The typical insertion loss is about –4.0 dB, and maximum less than –5.7 dB. This filter has a relatively high pass band ripple of about 1.0-1.5 dB, the largest insertion being at the high end of the band. The input and return losses are about –10 dB.

Power amplifier is 50Ω/50Ω module. It does not have its own enable/disable control signal, but it can be enabled by bias voltage and reference bias current signals. The gain window is +31 to +36 dB and linear output power is +30 dBm (typical condition) with -28 dB ACP. The nominal efficiency is 40 percent.

Power Control

For power monitoring, there is a power detector module (PDM) built from a (dual)coupler, a biased diode detector, and an NTC resistor. RF signals from both bands are routed via this PDM. The RF isolation between couplers is sufficient not to lose filtering performance given by duplex filters.

The diode output voltage and NTC voltage are routed to BB A/D converters for power control purposes. The TX AGC SW takes samples from diode output voltage and compares those values to target value, and adjusts BB I-and Q-signal amplitude and/or Safari PGA settings to keep power control in balance.

NTC voltage is used for diode temperature compensation and for thermal shutdown when radio board's temperature exceeds +85° C.

False TX indication is based on detected power measurement when carrier is not on.

The insertion loss of coupler is –0.42 dB (max) at cellular band and –0.48 dB (max) at PCS band. Typical values for insertion losses are about –0.2 dB. The filtering performance of diplexer is taken into account in system calculations.

Signal levels

Power Level	PGA	Pout
2	3	26.5/27.3
3	5	-4 dB
4	6	-4 dB
5	7	-4 dB
6	8	-4 dB
7	9	-4 dB
8	10	-4 dB
9	11	-4 dB
10	12	-4 dB

(For AMPS mode PL2 26.5 dBm, PL2 27.3 dBm for digital mode both bands)

Antenna Circuit

The antenna circuit consists of duplex filters, diplexer, three discrete matching components (C899, L899, L898)—which match the RF performance of the antenna—and an DCT3 RF connector/switch (X900). The maximum insertion loss is 0.3 dB.

Antenna

The NPW-2NX cellular antenna is an internal, dual-resonance planar, inverted F antenna (PIFA), mounted on a common dielectric substrate.